REMARKS/ARGUMENTS

The outstanding Office Action has rejected all claims 1-17 on various grounds and over five applied references (*Inumiya et al.* (USPN 6,054,355 hereinafter "*Inumiya*"), *Sugawara et al.* (USPN 6,841,430 hereinafter "*Sugawara*"), *Qiao et al.* (USPN 6,803,318 hereinafter "*Qiao*"), *Ma et al.* (USPN 6,759,695 hereinafter "*Ma*"), and *Divakaruni et al.* (USPN 6,501,131 hereinafter "*Divakaruni*"). **Claims 1, 16, & 17 are cancelled herein. Claims 2-7, 9-10, and 12 are amended.** The various ground of rejections are discussed below. The specification and various drawings are amended herein. New **Claims 18-25 are added. Claims 2-15 and 18-25 are now pending** in this application.

Rejection Under 35 U.S.C. § 102

Claims 1-3, 5-7, 10-11, and 16-17 have been rejected under 35 U.S.C. § 102(b) as being anticipated by *Inumiya*.

Claims 1, 16, and 17 have been cancelled making this ground of rejection moot as to those claims.

Claim 2 has been amended to include the limitations of independent Claim 1, it is otherwise unchanged in scope or subject matter. Claim 2 is rejected as anticipated by *Inumiya*. The applicants respectfully submit that the cited portions of *Inumiya* are insufficient to establish a *prima facie* case of anticipation and accordingly, the applicants traverse this rejection as follows.

Fig. 1G and Fig. 53B (and the supporting portions of the *Inumiya* Specification) are offered as anticipating Claim 2. **Fig. 1G** shows a process somewhat different and patentably distinct from the claimed invention. Claim 2 recites "etching a gate electrode trench ***in the first dielectric layer*** wherein the gate electrode trench etch stops on the underlying substrate" (emphasis added). Thus, in the claimed invention, the entire surface is covered with a first dielectric layer which is then etched through (in the gate region) to facilitate gate formation. This is not the case taught in Fig. 1G (or in supporting paragraphs dealing with layer 509). In *Inumiya*, the surface is patterned and a dummy gate pattern 505 is formed (e.g., *Inumiya* 1:40-45). Nitride sidewalls 507 (e.g., *Inumiya* 1:50-54, 2:45-3:10) are then formed for the dummy gate 505. The claimed invention does not used

the process of dummy gate creation. Then a CVD-SiO_2 film 509 is formed and flattened (e.g., *Inumiya* 1:60-65). This layer 509 is described in the Office Action as the first dielectric layer. As an aside, these descriptions were given to illustrate the problems in the prior art. The same problems that the process changes of the claimed invention remedy by an alternative process approach. However, it is the next step in *Inumiya* that the differences from the prior art process become very clear from the claimed invention. The cited art then removes the dummy material 505 from the gate area. The claimed invention does no such process. The claimed invention does not uses the dummy gate formation process, but rather etches directly through the first dielectric layer to define the gate contact region. This is different from the cited portion of *Inumiya* which teaches that the opening is made not in the first dielectric layer 509 but rather in the dummy gate material 505 (See, e.g., *Inumiya* Figs. 1F, 1G, and the supporting portions of the Spec.). Thus, at a fundamental level, the cited portion of *Inumiya* fail to teach the limitation of etching through the dielectric layer. Accordingly, the cited portion of *Inumiya* fails to establish a *prima facie* case of anticipation by omitting a key process step needed in the claimed invention.

Additionally, **Fig. 52B** shows a process that is also somewhat different and patentably distinct from the claimed invention. Claim 2 recites "etching a gate electrode trench in the first dielectric layer ***wherein the gate electrode trench etch stops on the underlying substrate***" (emphasis added). In the process outlined in the cited portions of *Inumiya* (e.g., Figs. 52A, 52B, 53A, 53B, 54A, 54B, 55A, 55B, 56A, 56B, 57A, and 57B) the process does not stop when it reaches the underlying substrate 61 but rather continues on etching into and beneath the substrate rather than stopping on the substrate as claimed. Additionally, Claim 2 recites "depositing a conformal gate dielectric film to line the trench". It is offered that *Inumiya* teaches this limitation (*Inumiya* at Figs. 54-56 and 38:1-32). The applicants believe this not to be the case. The cited layer 69 is a thermally grown oxide rather than a deposited high-K material (this particular point is made more clearly in amended Claim 5). The grown oxide can only grow on the areas where the silicon is exposed or a nitride layer is formed. In Fig. 54B it is clear that the oxide is grown over the exposed substrate portion, but not the ILD sidewalls of the trench. Thus, only a portion of the substrate is oxided by thermal oxide growth rather than the entire trench being grown by means of a conformal deposition process as is claimed.

Thus, for at least these reasons, the applicants respectfully submit that the cited portions of the art fail to teach all claim elements of the claimed invention. Accordingly, the cited portions of the prior art do not establish a *prima facie* case for anticipation and are therefore insufficient to establish a rejection under 35 U.S.C. § 102. Therefore, the applicants respectfully request that this ground of rejection be withdrawn as to **Claim 2.**

Additionally, as amended **Claims 5-7 and 10-11** depend on Claim 2, which is believed allowable for at least the forgoing reasons. The applicants believe that the underlying claims are allowable for a number of reasons. However, due to the believed allowability of the base claim, applicants need not discuss the additional reasons for allowing the dependent claims at this time. Accordingly, the applicants respectfully request the withdrawal of the rejected dependent claims.

Claim 3 has been amended to include the limitations of independent Claim 1, additionally it includes a limitation specifying that the gate electrode etch step forms "a trench extension into the substrate that extends into the substrate a depth sufficient to include an ***entire device inversion channel***" (emphasis added). This claim amendment clarifies the depth of the etch. It is conducted so that the subsequently formed epitaxial layers contain the entire inversion channel. This is different from the cited art which requires that the inversion channel be underneath, or at least partially underneath, the electrode. See, the channel 68 indicated in Figs. 54-56 of *Inumiya*. The applicants believe that this and other limitations distinguish the cited art from the claimed invention. Thus, for at least these reasons, the applicants respectfully submit as amended Claim 3 overcomes the anticipation rejection set forth in the teachings of *Inumiya* and therefore, the applicants respectfully request that this ground of rejection be withdrawn as to **Claim 3.**

Rejections Under 35 U.S.C. § 103

Claims 4, 8-9, and 12-15 stand rejected as unpatentable under 35 U. S. C. §§ 103(a) in view of numerous references. These references and rejections are discussed in detail below.

Claim 4 is rejected as unpatentable over *Inumiya* in view of *Qiao*. Claim 4 is dependent on Claim 2. The rejection of claim 2 over *Inumiya* has been discussed in detail hereinabove. Nothing in the cited portions of *Qiao* remedies the deficiencies in *Inumiya* explained above. Accordingly, for at least the reasons explained above with respect to base claim 2, the applicants submit that the

cited combination of references is insufficient to establish a *prima facie* case of obviousness as to Claim 4. Accordingly, applicants respectfully request that the pending ground of rejection for Claim 4 be withdrawn.

Claims 8-9 are rejected as unpatentable over *Inumiya* in view of *Divakaruni*. Claims 8 and 9 are dependent on Claim 2. The rejection of claim 2 over *Inumiya* has been discussed in detail hereinabove. Nothing in the cited portions of *Qiao* remedies the deficiencies in *Inumiya* explained above. Accordingly, for at least the reasons explained above with respect to base claim 2, the applicants submit that the cited combination of references is insufficient to establish a *prima facie* case of obviousness as to Claims 8-9. Accordingly, applicants respectfully request that the pending ground of rejection for Claim 8 and 9 be withdrawn.

Claims 12-15 are rejected as unpatentable over *Inumiya* in view of *Sugawara* or *Ma*. Claims 12-15 are dependent on Claim 3. The rejection of claim 3 over *Inumiya* has been discussed in detail hereinabove. Nothing in the cited portions of *Sugawara* or *Ma* remedies the deficiencies in *Inumiya* explained above.

Moreover, as to **Claim 14** specifically, none of the references reference teaches the limitation of an epitaxially grown silicon layer that is "a strained silicon layer formed on a Ge layer grown in the channel trench".

Accordingly, for at least the reasons explained above with respect to base claim 3, the applicants submit that the cited combination of references is insufficient to establish a *prima facie* case of obviousness as to Claims 12-15. Accordingly, applicants respectfully request that the pending ground of rejection for Claims 12-15 be withdrawn.

The applicants point out that no art induced amendment have been made to Claim 2 which has the same scope as prior to amendment and that no new matter is added to this Claim.

New Claims:

Claims 18-25 have been added to specifically clarify certain patentable subject matter. Of particular relevance is the post anneal and implantation operations of gate formation and dielectric layer formation. Such operations are embodied, for example, by **Claim 18** "after forming the source and drain diffusion region and after annealing, covering the surface of the semiconductor substrate with a first layer of dielectric material to form a first interlayer dielectric layer on the semiconductor

substrate after formation of the source and drain diffusions". The specific advantages of such sequencing include an enhanced thermal budget and other process advantages described in the specification. Moreover, the underlying art is believed to be insufficient for the reasons discussed above with respect to the other claims.

Conclusion:

In view of the foregoing amendments and remarks, it is respectfully submitted that the claimed invention as presently presented is patentable over the art of record and that this case is now in condition for allowance.

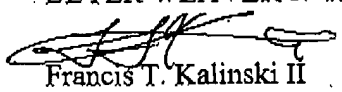
Accordingly, the applicants request withdrawal of all pending rejections and request reconsideration of the pending application and prompt passage to issuance. As an aside, the applicants clarify that any lack of response to any of the issues raised by the Examiner is not an admission by the applicant as to the accuracy of the Examiner's assertions with respect to such issues. Accordingly, applicant's specifically reserve the right to respond to such issues at a later time during the prosecution of the present application, should such a need arise.

As always, the Examiner is cordially invited to telephone the applicants representative to discuss any matters pertaining to this case. Should the Examiner wish to contact the undersigned for any reason, the telephone numbers set out below can be used.

Additionally, if any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 12-2252 (Order No. 03-2051).

Respectfully submitted,

BEYER WEAVER & THOMAS, LLP



Francis T. Kalinski II
Registration No. 44,177

P.O. Box 70250
Oakland, CA 94612-0250
Telephone: (831) 642-9609
Alt. Tel.: (650) 961-8300